DOCKET NO. 99-2760

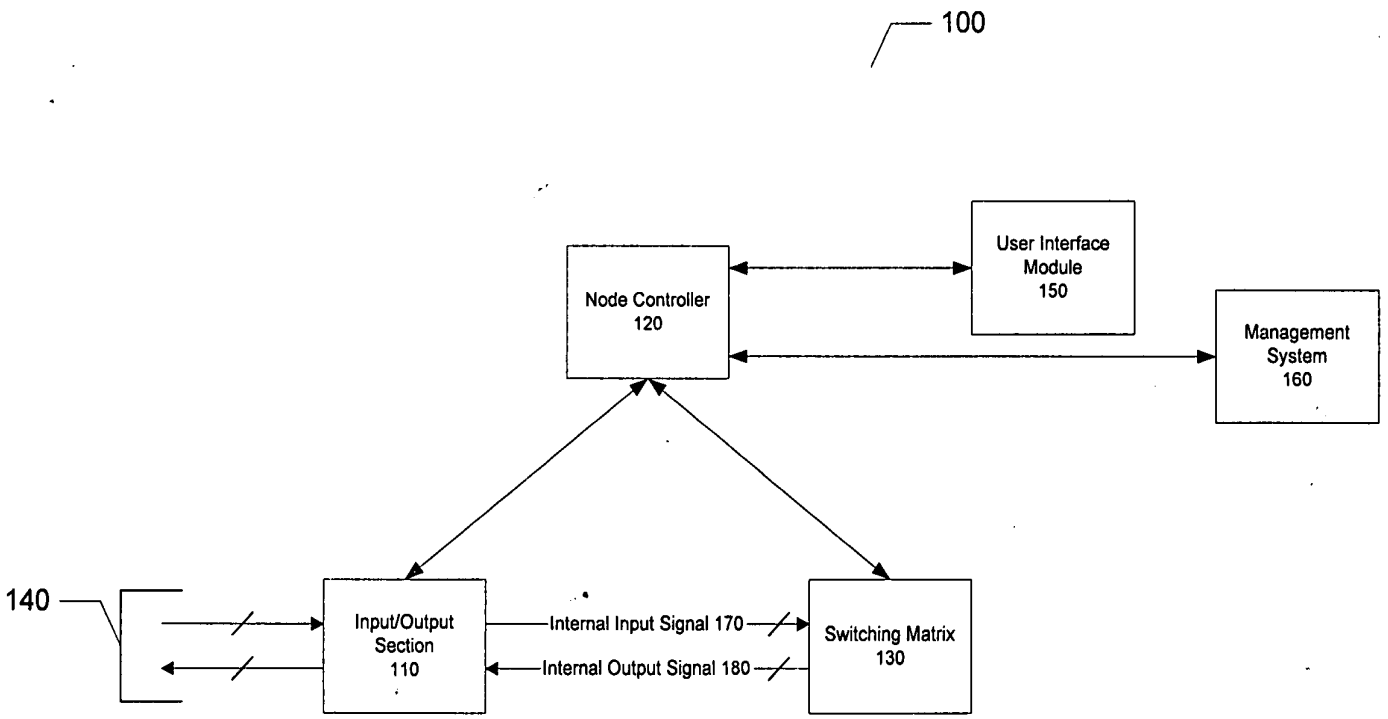

Fig. 1A

00h0T0" 99t2Zh60

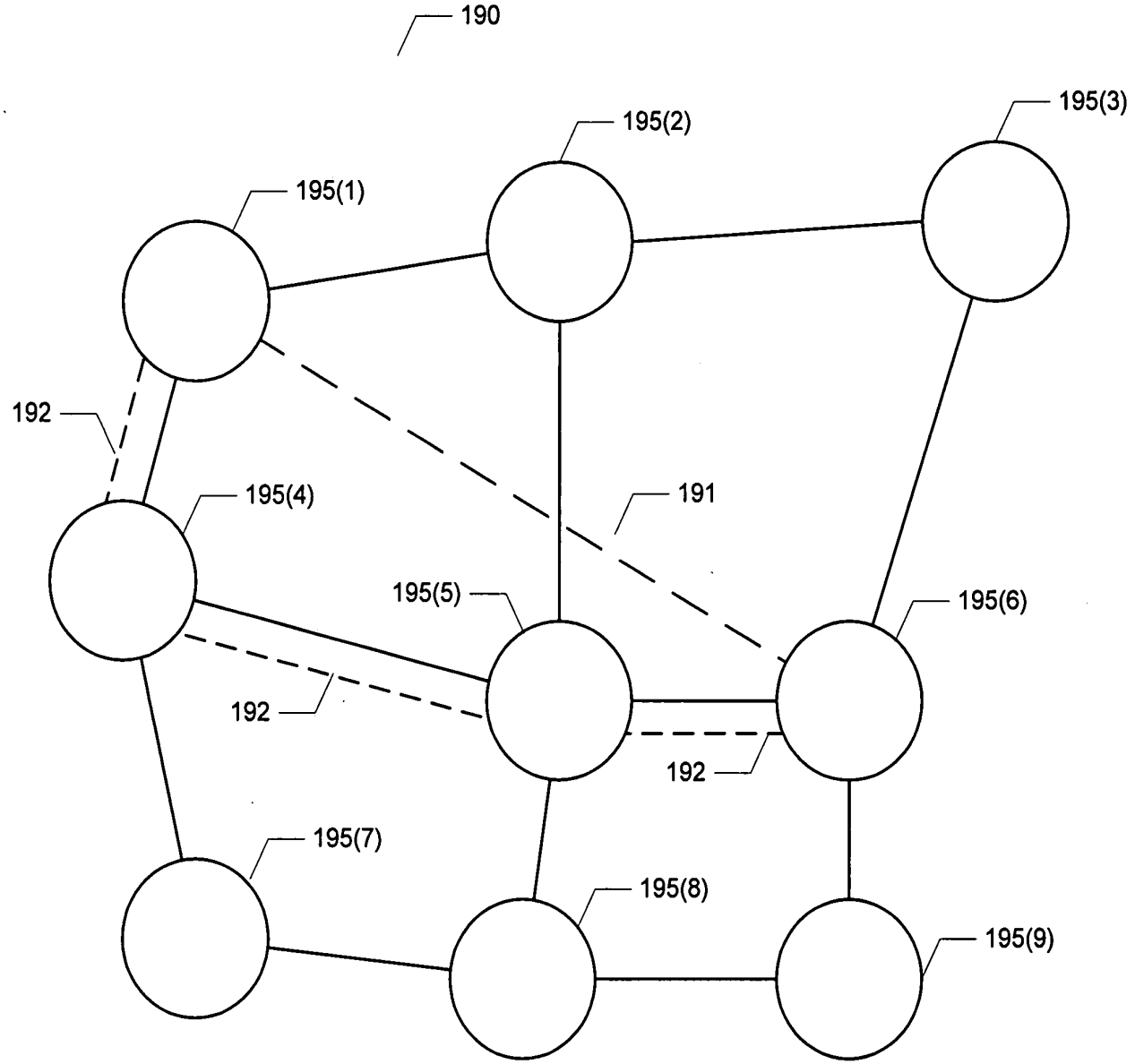

Fig. 1B

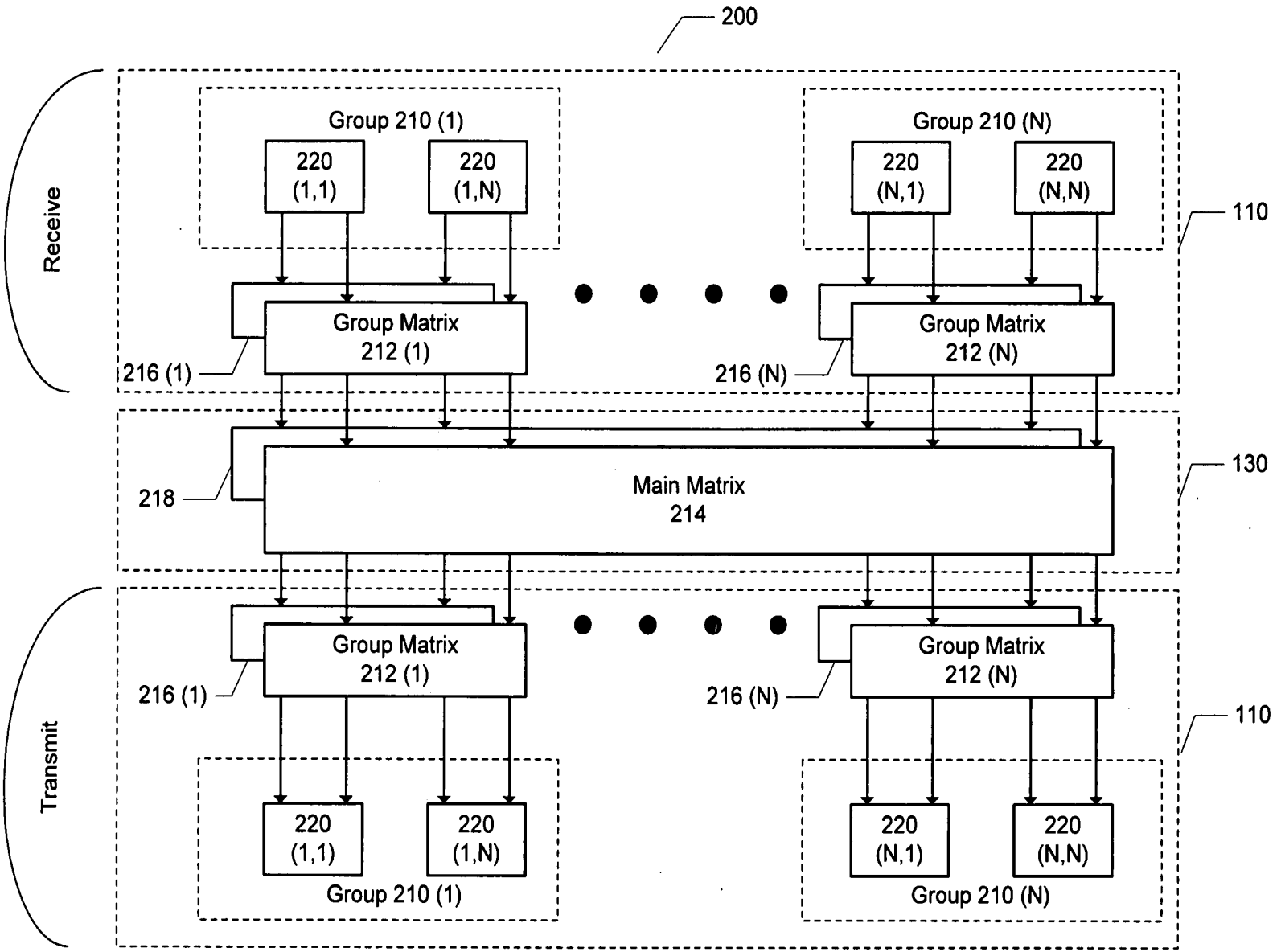
200
Receive
Group 210 (1)
220 (1,1)
220 (1,N)
Group 210 (N)
220 (N,1)
220 (N,N)
110
Group Matrix 212 (1)
Group Matrix 212 (N)
216 (1)
216 (N)
218
Main Matrix 214
130
Transmit
Group Matrix 212 (1)
Group Matrix 212 (N)
216 (1)
216 (N)
110
220 (1,1)
220 (1,N)
220 (N,1)
220 (N,N)
Group 210 (1)
Group 210 (N)

Fig. 2

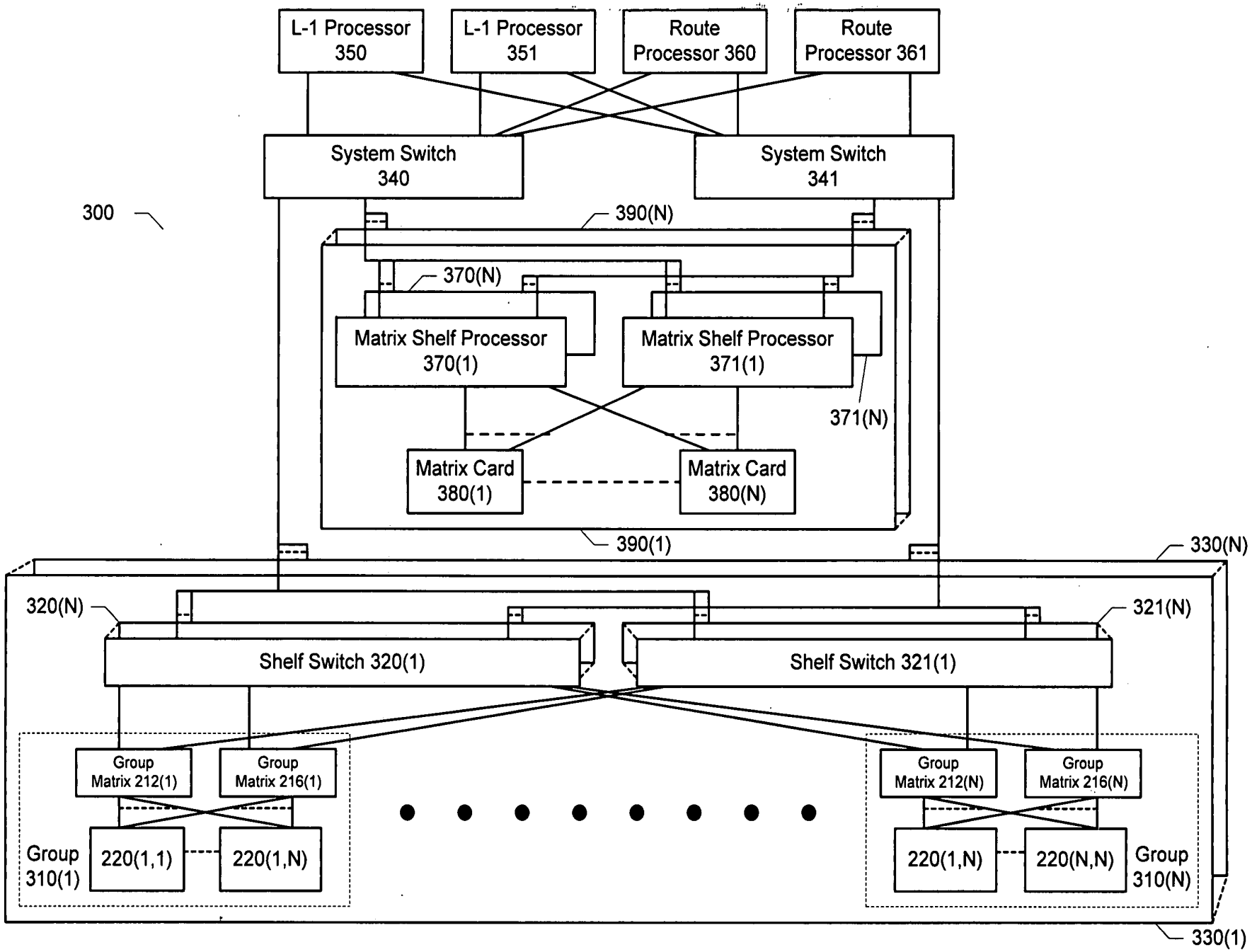
L-1 Processor 350
L-1 Processor 351
Route Processor 360
Route Processor 361
System Switch 340
System Switch 341
300
390(N)
370(N)
Matrix Shelf Processor 370(1)
Matrix Shelf Processor 371(1)
371(N)
Matrix Card 380(1)
Matrix Card 380(N)
390(1)
330(N)
320(N)
321(N)
Shelf Switch 320(1)
Shelf Switch 321(1)
Group Matrix 212(1)
Group Matrix 216(1)
Group Matrix 212(N)
Group Matrix 216(N)
Group 310(1)
220(1,1)
220(1,N)
220(1,N)
220(N,N)
Group 310(N)
330(1)

Fig. 3

09h77h60 '99T77h60

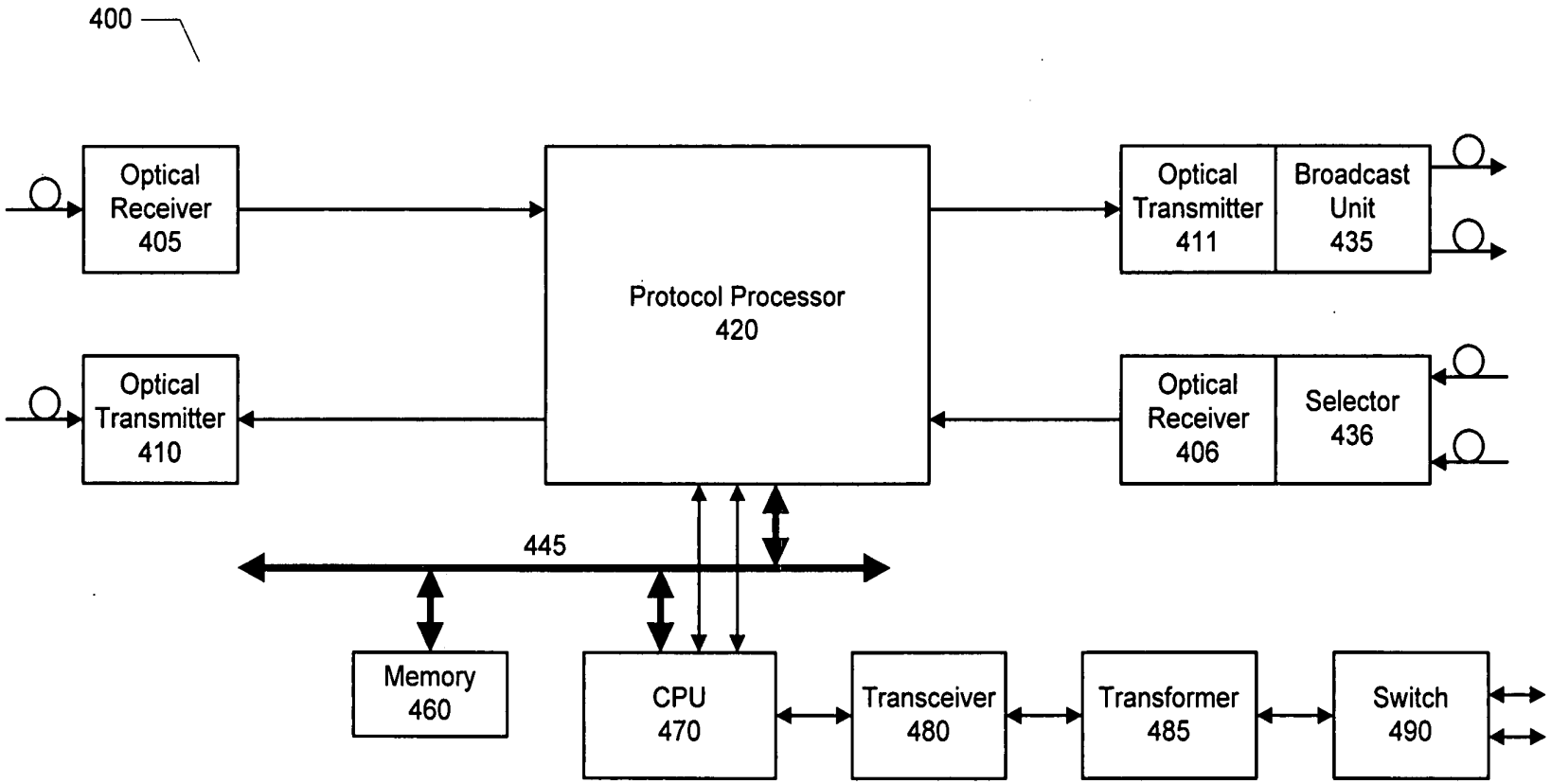

Fig. 4

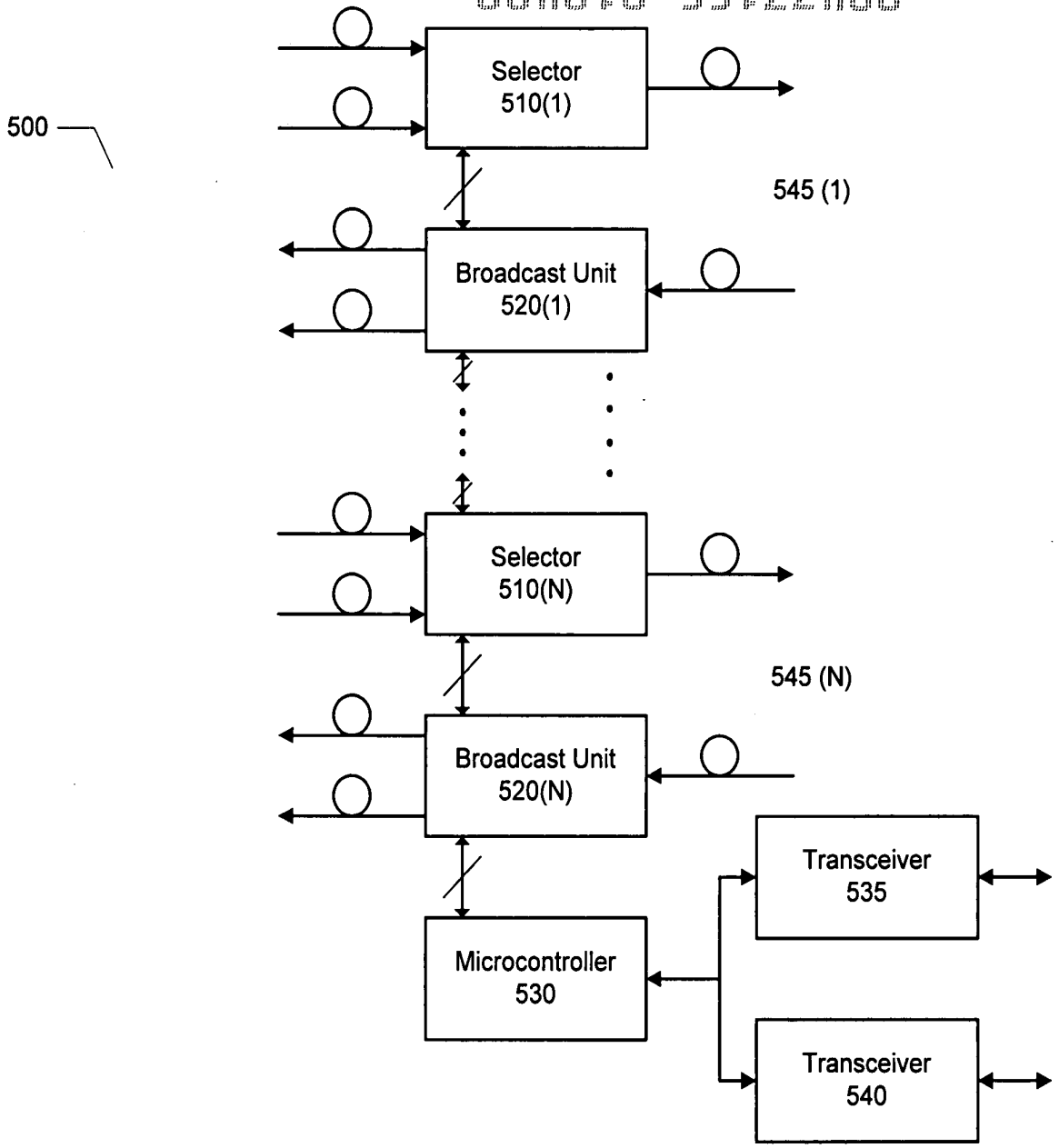
500
Selector
510(1)
545 (1)
Broadcast Unit
520(1)
Selector
510(N)
545 (N)
Broadcast Unit
520(N)
Transceiver
535
Microcontroller
530
Transceiver
540

Fig. 5

DOMOTO 99727760

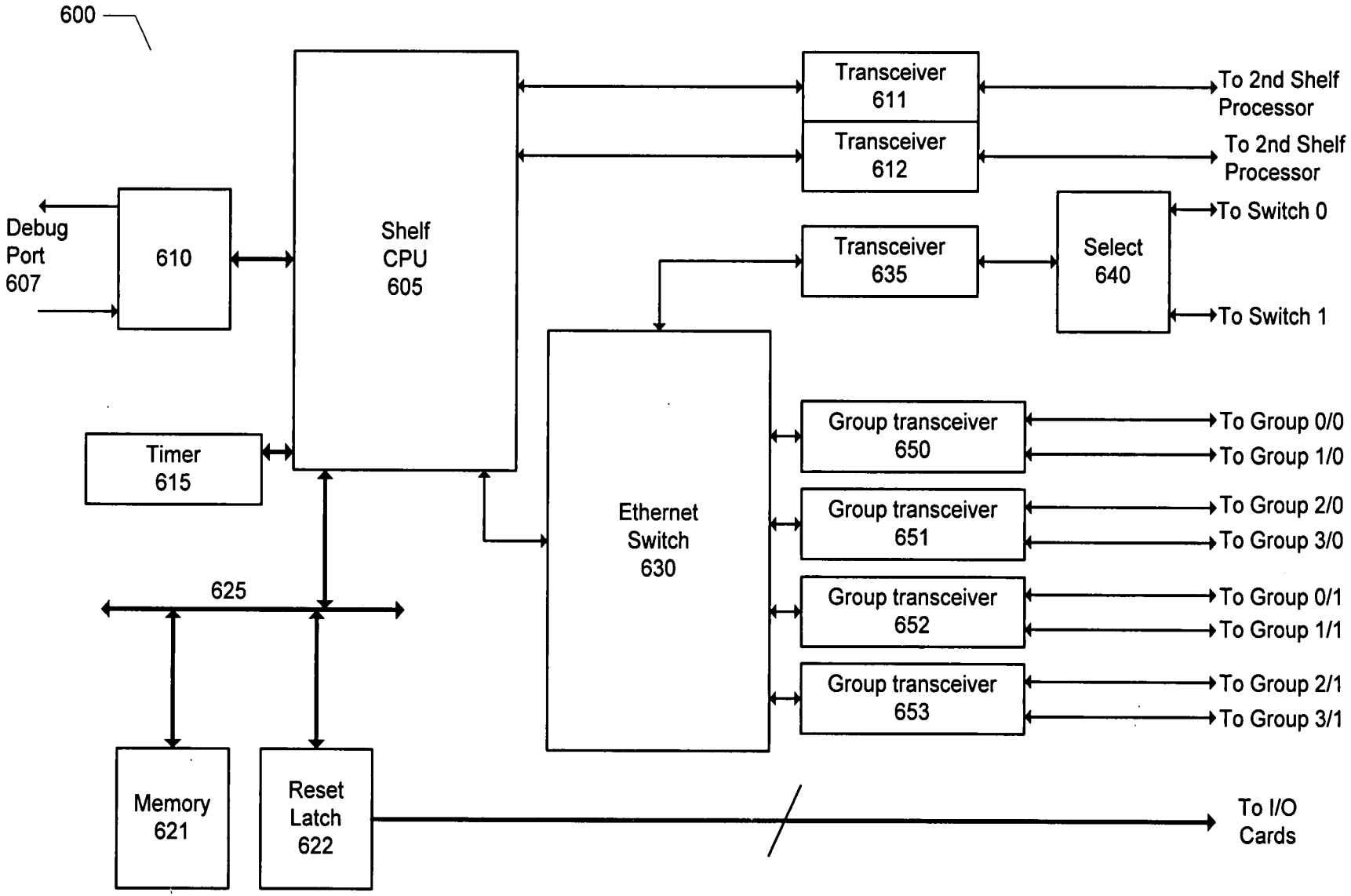

Fig. 6

00h070 9972h60

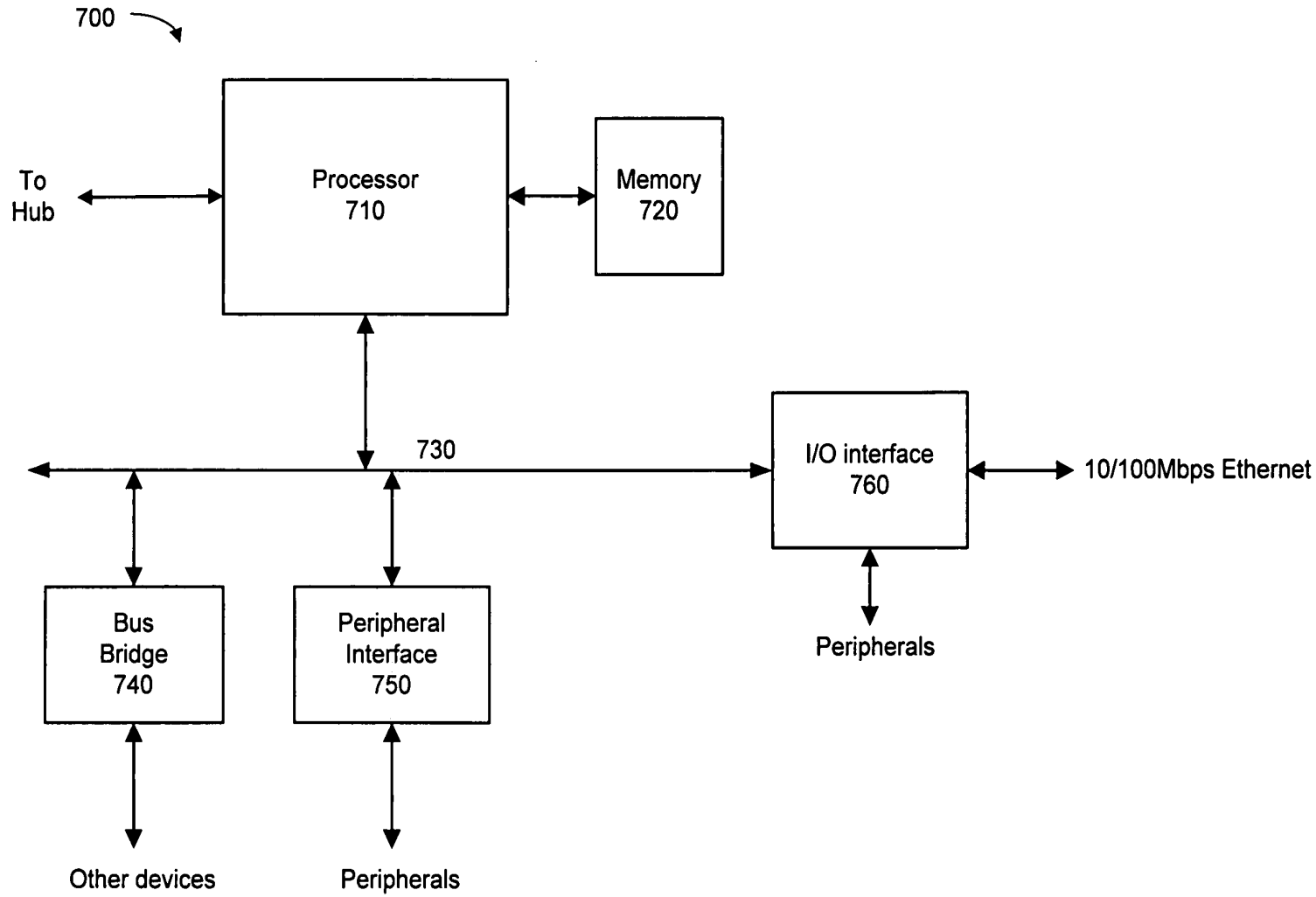

Fig. 7

00n0T0" 99T24n60

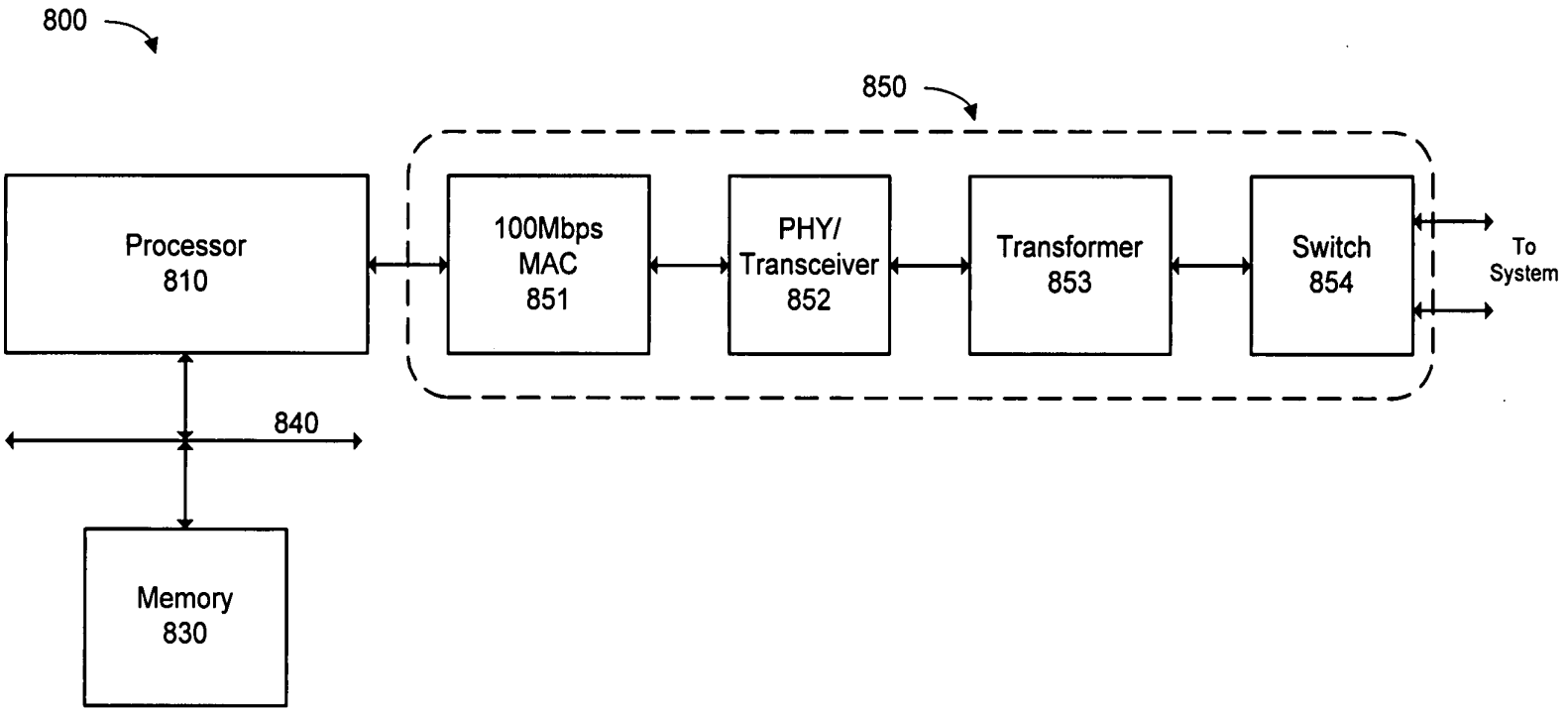

Fig. 8

09h727h56 .0Th0D

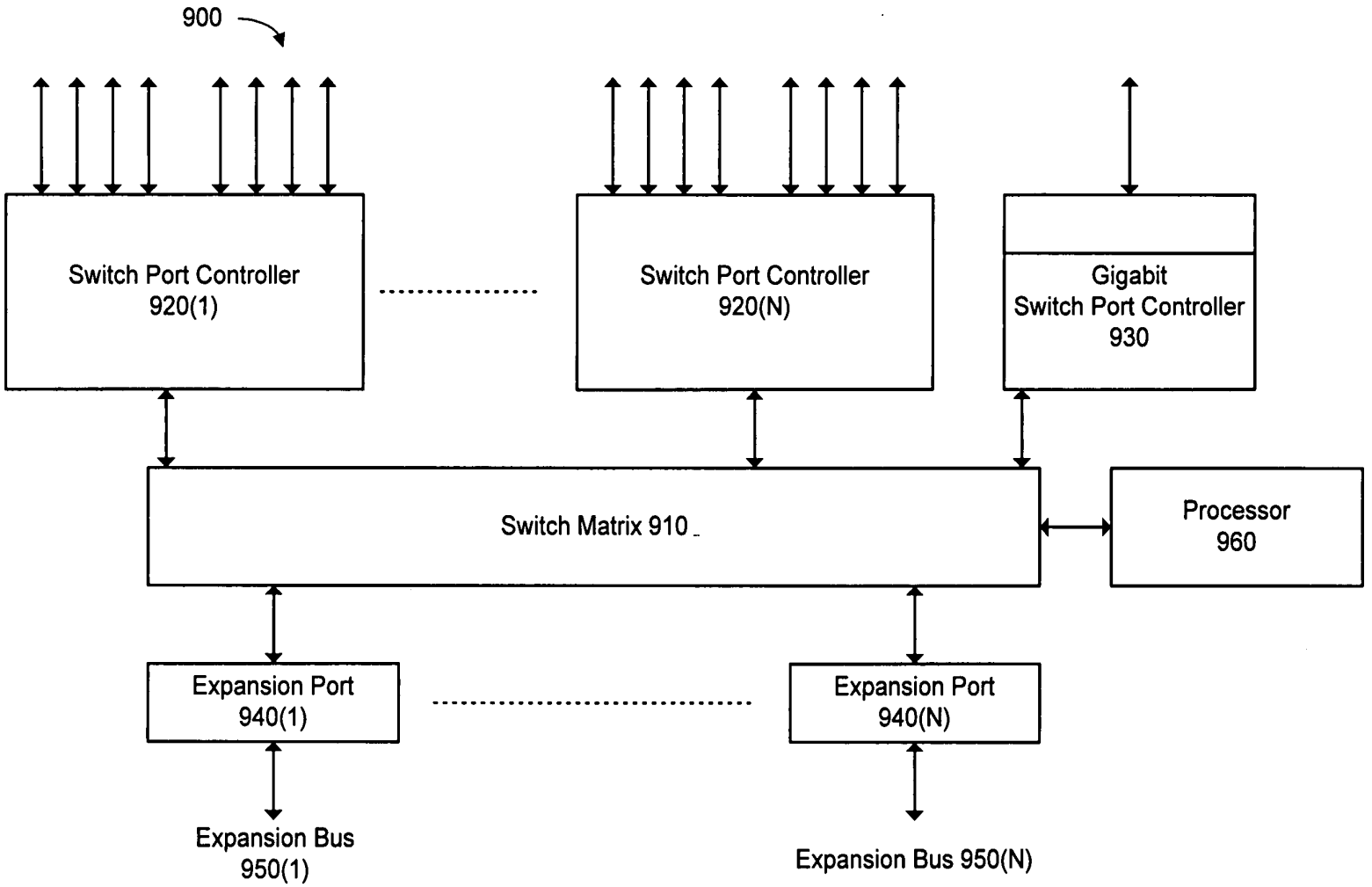

Fig. 9

DOCKET NO. 99-2760

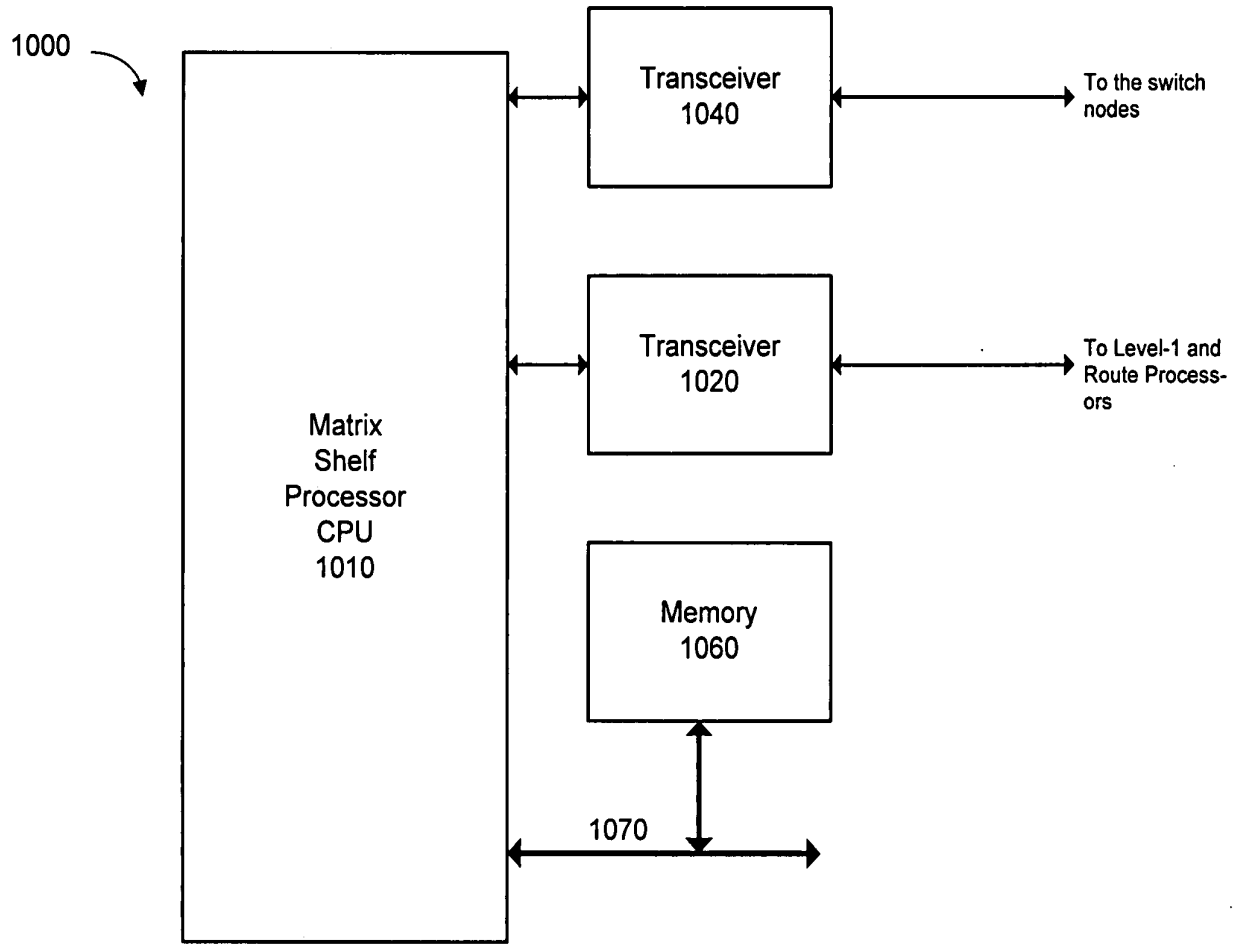

Fig. 10

DOMOTO" 99T2760

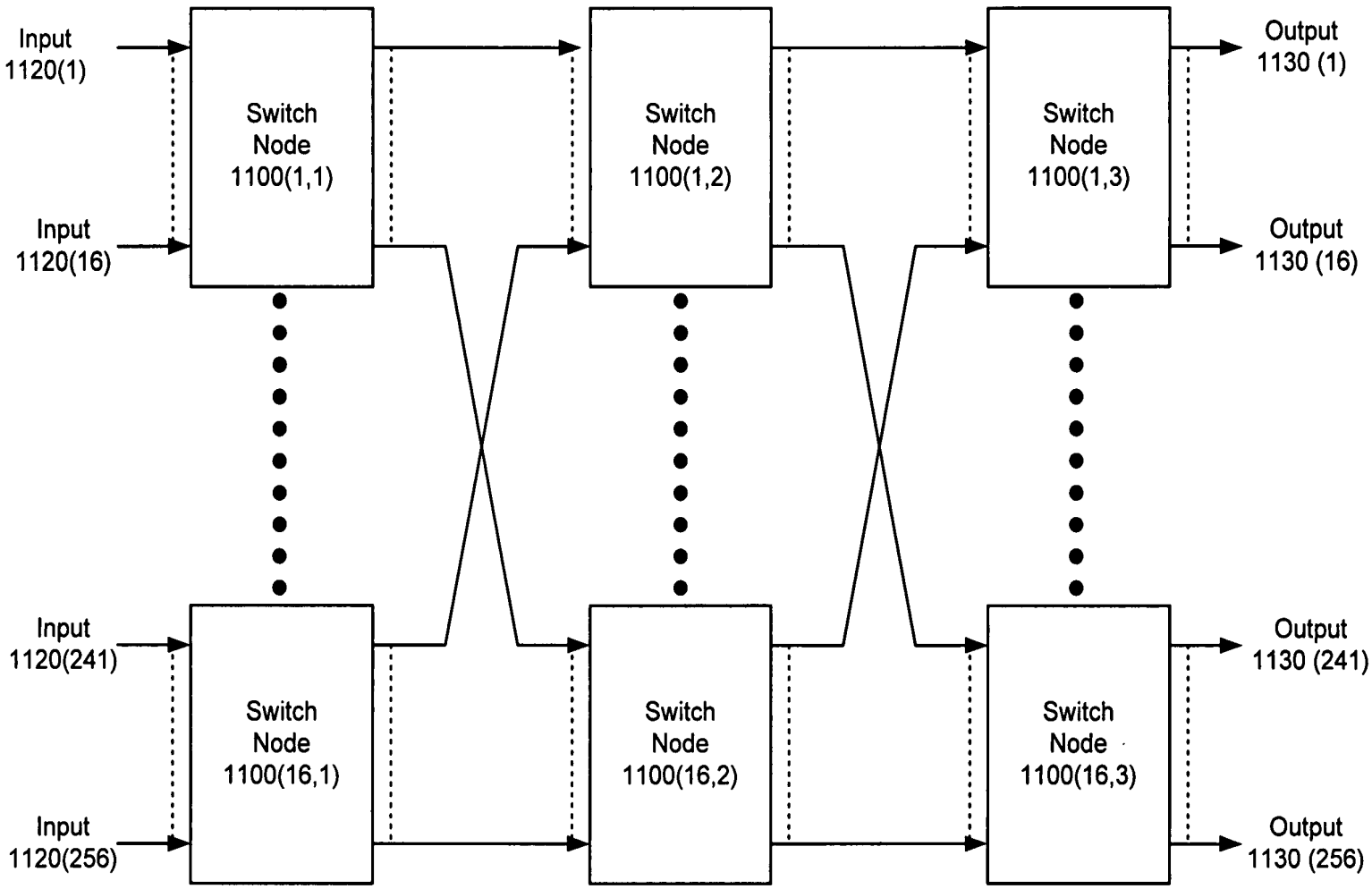

Fig. 11

00h0T0" 99T2Zh60

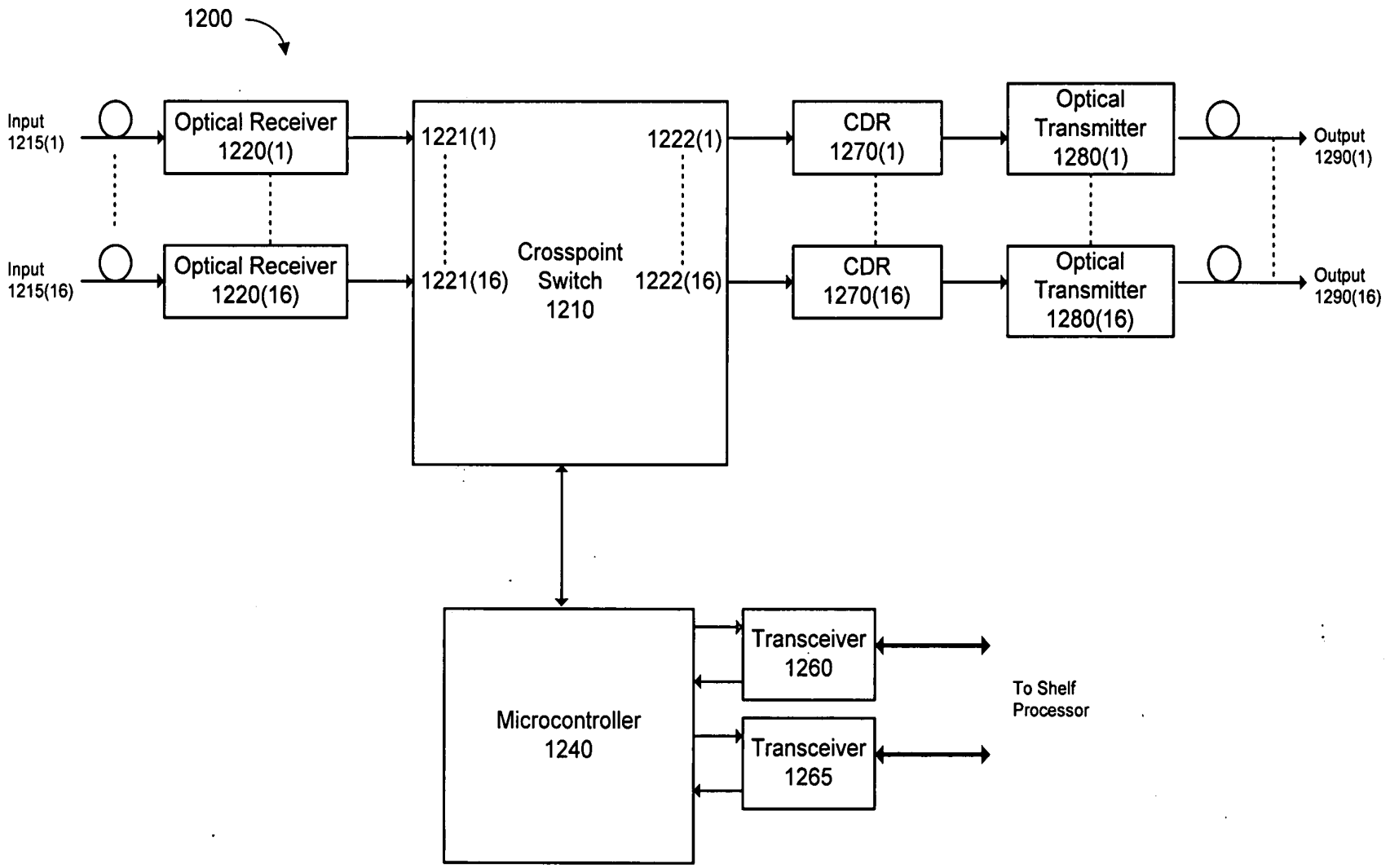

Fig. 12

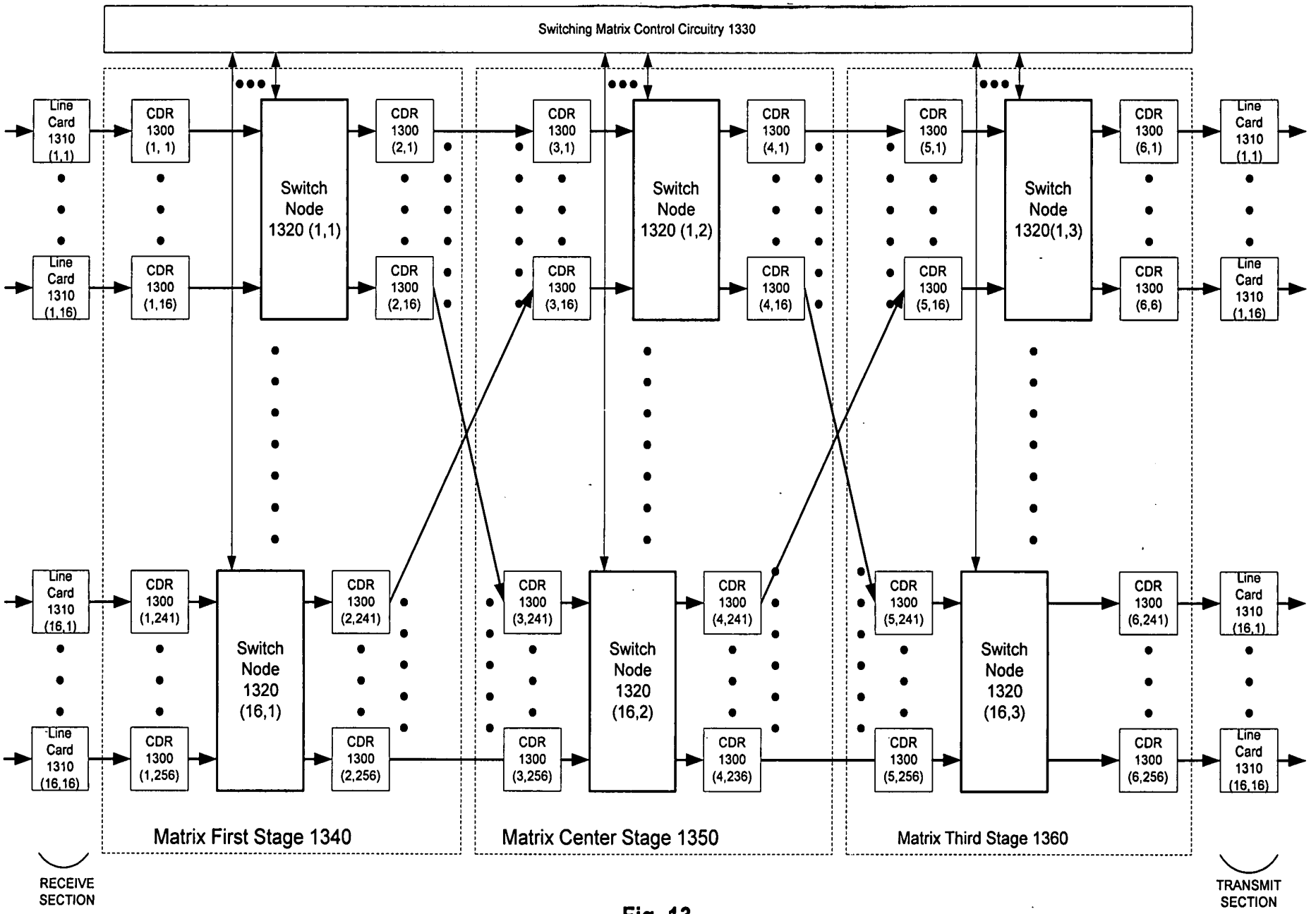
Switching Matrix Control Circuitry 1330
Line Card 1310 (1,1)
Line Card 1310 (1,16)
Line Card 1310 (16,1)
Line Card 1310 (16,16)
CDR 1300 (1, 1)
CDR 1300 (1,16)
CDR 1300 (1,241)
CDR 1300 (1,256)
Switch Node 1320 (1,1)
Switch Node 1320 (16,1)
CDR 1300 (2,1)
CDR 1300 (2,16)
CDR 1300 (2,241)
CDR 1300 (2,256)
CDR 1300 (3,1)
CDR 1300 (3,16)
CDR 1300 (3,241)
CDR 1300 (3,256)
Switch Node 1320 (1,2)
Switch Node 1320 (16,2)
CDR 1300 (4,1)
CDR 1300 (4,16)
CDR 1300 (4,241)
CDR 1300 (4,236)
CDR 1300 (5,1)
CDR 1300 (5,16)
CDR 1300 (5,241)
CDR 1300 (5,256)
Switch Node 1320(1,3)
Switch Node 1320 (16,3)
CDR 1300 (6,1)
CDR 1300 (6,6)
CDR 1300 (6,241)
CDR 1300 (6,256)
Line Card 1310 (1,1)
Line Card 1310 (1,16)
Line Card 1310 (16,1)
Line Card 1310 (16,16)
Matrix First Stage 1340
Matrix Center Stage 1350
Matrix Third Stage 1360
RECEIVE SECTION
TRANSMIT SECTION

Fig. 13

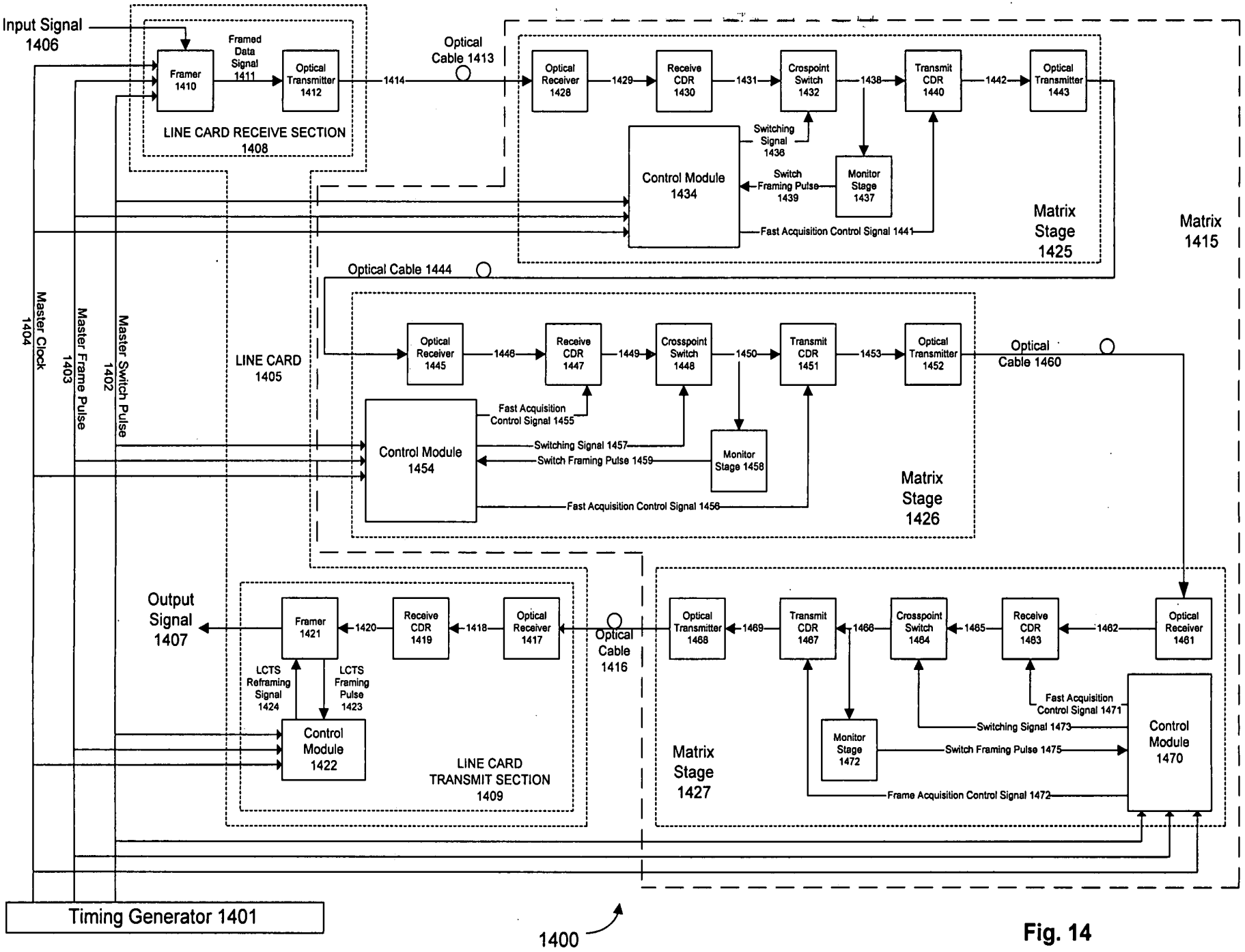
Input Signal 1406
Framer 1410
Framed Data Signal 1411
Optical Transmitter 1412
LINE CARD RECEIVE SECTION 1408
1414
Optical Cable 1413
Optical Receiver 1428
1429
Receive CDR 1430
1431
Crospoint Switch 1432
1438
Transmit CDR 1440
1442
Optical Transmitter 1443
Switching Signal 1436
Control Module 1434
Switch Framing Pulse 1439
Monitor Stage 1437
Fast Acquisition Control Signal 1441
Matrix Stage 1425
Matrix 1415
Optical Cable 1444
Master Clock 1404
Master Frame Pulse 1403
Master Switch Pulse 1402
LINE CARD 1405
Optical Receiver 1445
1446
Receive CDR 1447
1449
Crosspoint Switch 1448
1450
Transmit CDR 1451
1453
Optical Transmitter 1452
Optical Cable 1460
Fast Acquisition Control Signal 1455
Control Module 1454
Switching Signal 1457
Switch Framing Pulse 1459
Monitor Stage 1458
Fast Acquisition Control Signal 1456
Matrix Stage 1426
Output Signal 1407
Framer 1421
1420
Receive CDR 1419
1418
Optical Receiver 1417
Optical Cable 1416
Optical Transmitter 1468
1469
Transmit CDR 1467
1466
Crosspoint Switch 1464
1465
Receive CDR 1463
1462
Optical Receiver 1461
LCTS Reframing Signal 1424
LCTS Framing Pulse 1423
Control Module 1422
LINE CARD TRANSMIT SECTION 1409
Fast Acquisition Control Signal 1471
Switching Signal 1473
Monitor Stage 1472
Switch Framing Pulse 1475
Control Module 1470
Matrix Stage 1427
Frame Acquisition Control Signal 1472
Timing Generator 1401
1400

Fig. 14

SONET Frame
1500

A1 1502	A2 1504	J0 Z0 1506 U	Payload Bytes 1590	
B1 1510	E1 U 1512	F1 U 1514	Payload Bytes 1591	
D1 U 1520	D2 U 1522	D3 U 1524	Payload Bytes 1592	
H1 1530	H2 1532	H3 1534	H4 1536	Payload Bytes 1593
B2 U 1540	K1 U 1542	K2 U 1544	Payload Bytes 1594	
D4 U 1550	D5 U 1551	D6 U 1552	Payload Bytes 1595	
D7 U 1553	D8 U 1554	D9 U 1555	Payload Bytes 1596	
D10 U 1556	D11 U 1557	D12 U 1558	Payload Bytes 1597	
S1 Z1 1570 U	M1 Z2 1572 U	E2 U 1574	Payload Bytes 1598	

Fig. 15
(Prior Art)

DOMOTO 99E2760

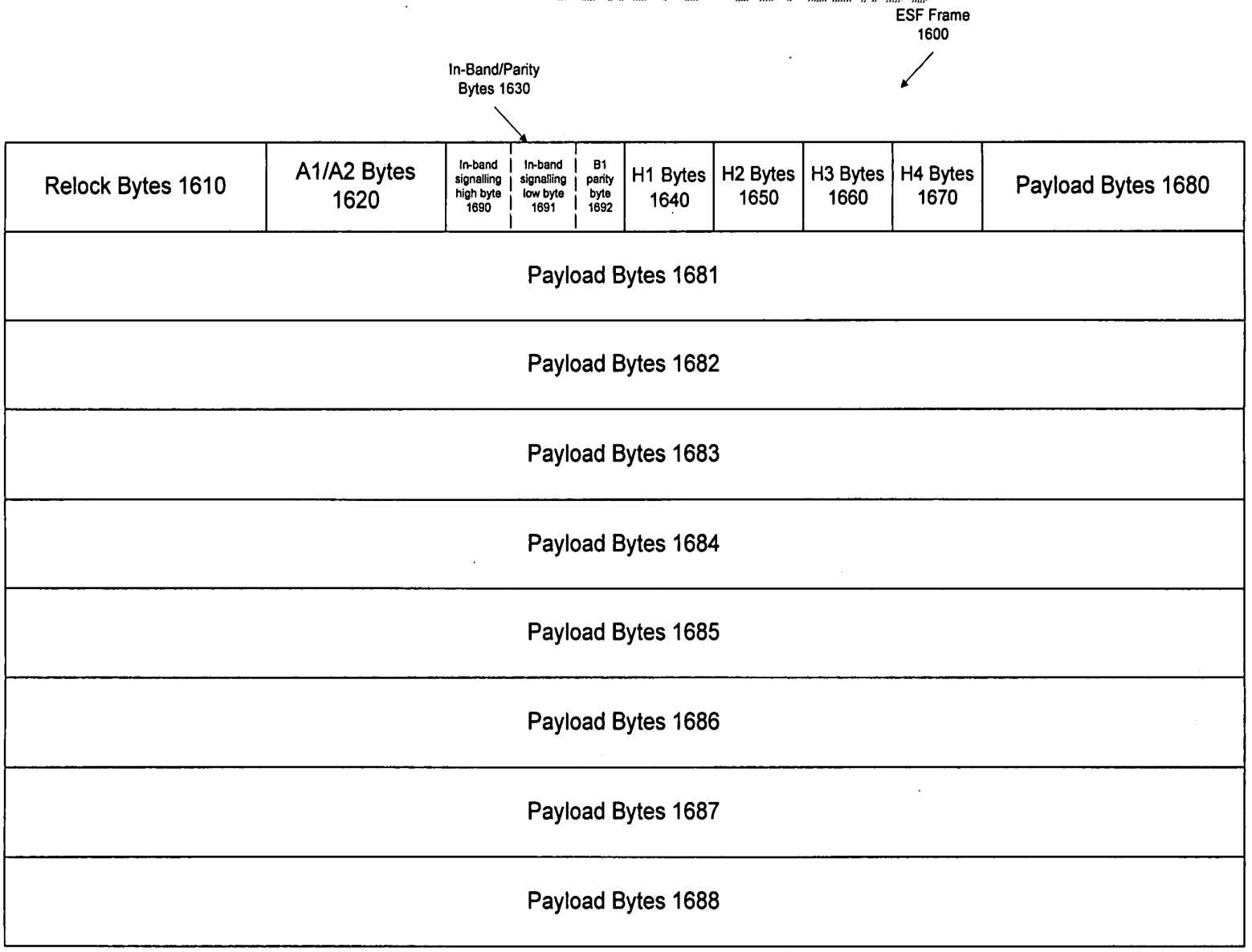

Fig. 16

Master Frame Pulse 1403
Master Switch Pulse 1402
Framed Data Signal 1411
DATA
55
F
DATA
Signal 1429, 1431
Switching Signal 1436
Signal 1438
Switch Framing Pulse 1439
Fast Acquisition Control Signal 1441
Signal 1442
Signal 1446
Fast Acquisition Control Signal 1455
Signal 1449
Switching Signal 1457
Signal 1450
Switch Framing Pulse 1459
Fast Acquisition Control Signal 1456
Signal 1453
Signal 1462
Fast Acquisition Control Signal 1471
Signal 1465
Switching Signal 1473
Signal 1466
Switch Framing Pulse 1475
Fast Acquisition Control Signal 1472
Signal 1469
Signal 1418
Signal 1420
LCTS Reframing Signal 1424

Fig. 17

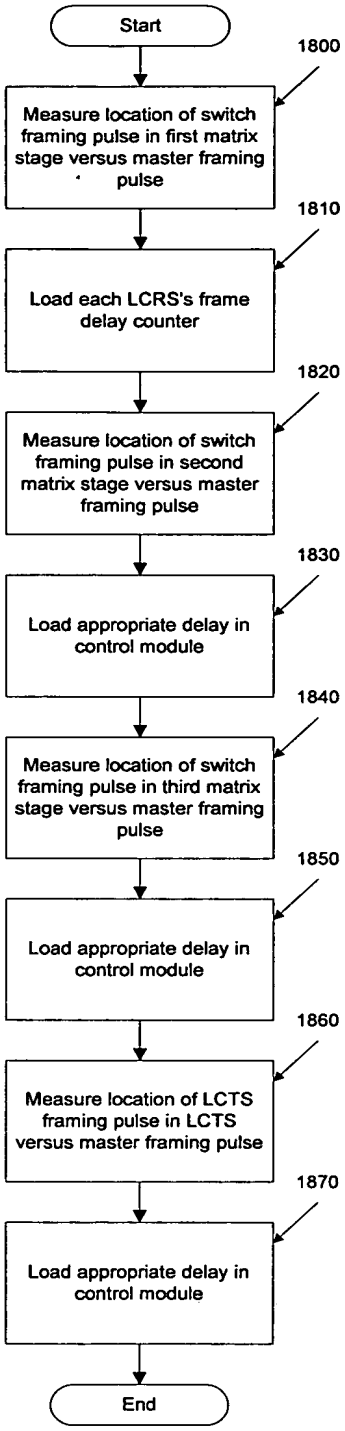
Start
1800
Measure location of switch framing pulse in first matrix stage versus master framing pulse
1810
Load each LCRS's frame delay counter
1820
Measure location of switch framing pulse in second matrix stage versus master framing pulse
1830
Load appropriate delay in control module
1840
Measure location of switch framing pulse in third matrix stage versus master framing pulse
1850
Load appropriate delay in control module
1860
Measure location of LCTS framing pulse in LCTS versus master framing pulse
1870
Load appropriate delay in control module
End

Fig. 18

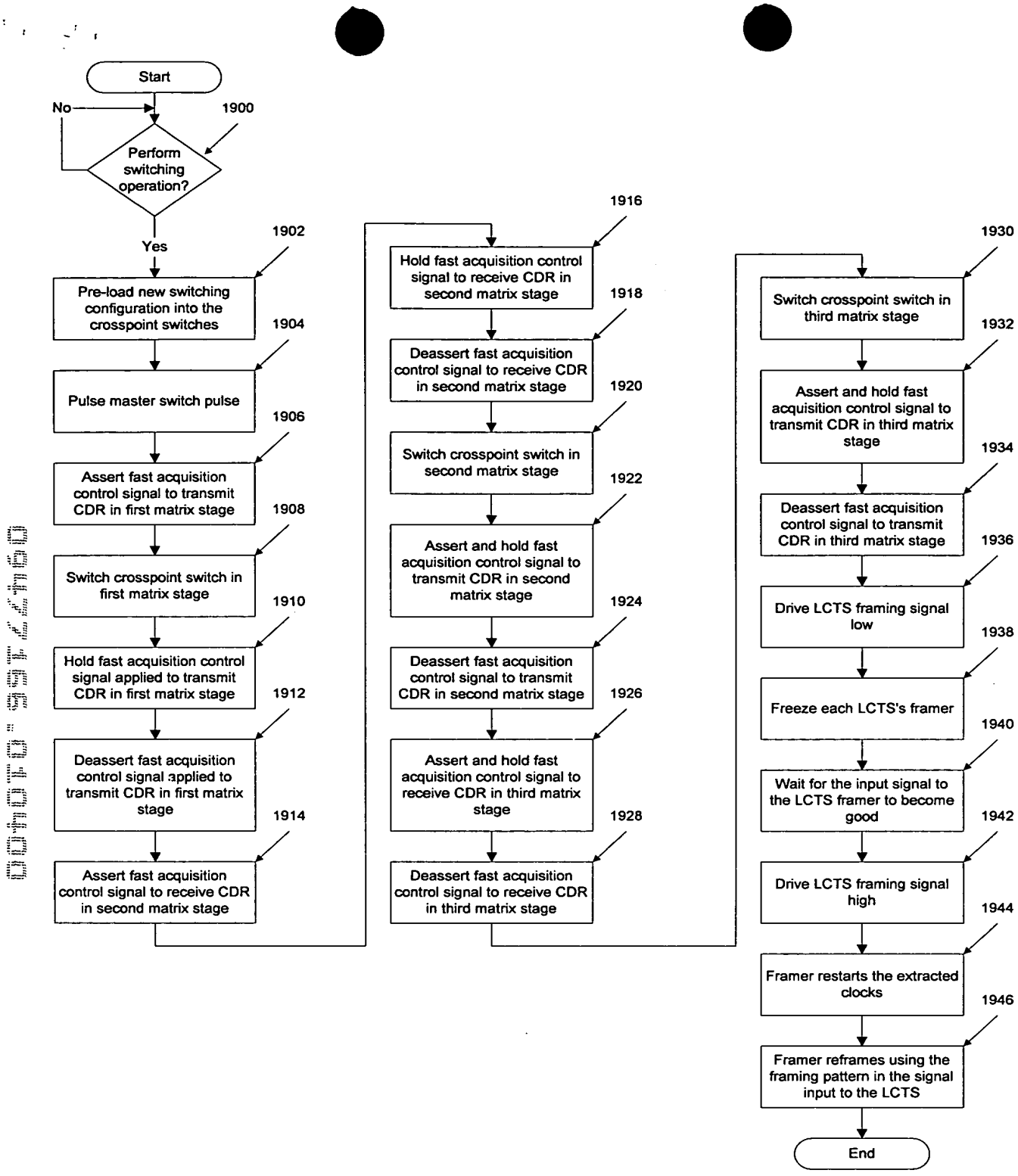
Start
No
1900
Perform switching operation?
Yes
1902
Pre-load new switching configuration into the crosspoint switches
1904
Pulse master switch pulse
1906
Assert fast acquisition control signal to transmit CDR in first matrix stage
1908
Switch crosspoint switch in first matrix stage
1910
Hold fast acquisition control signal applied to transmit CDR in first matrix stage
1912
Deassert fast acquisition control signal applied to transmit CDR in first matrix stage
1914
Assert fast acquisition control signal to receive CDR in second matrix stage
1916
Hold fast acquisition control signal to receive CDR in second matrix stage
1918
Deassert fast acquisition control signal to receive CDR in second matrix stage
1920
Switch crosspoint switch in second matrix stage
1922
Assert and hold fast acquisition control signal to transmit CDR in second matrix stage
1924
Deassert fast acquisition control signal to transmit CDR in second matrix stage
1926
Assert and hold fast acquisition control signal to receive CDR in third matrix stage
1928
Deassert fast acquisition control signal to receive CDR in third matrix stage
1930
Switch crosspoint switch in third matrix stage
1932
Assert and hold fast acquisition control signal to transmit CDR in third matrix stage
1934
Deassert fast acquisition control signal to transmit CDR in third matrix stage
1936
Drive LCTS framing signal low
1938
Freeze each LCTS's framer
1940
Wait for the input signal to the LCTS framer to become good
1942
Drive LCTS framing signal high
1944
Framer restarts the extracted clocks
1946
Framer reframes using the framing pattern in the signal input to the LCTS
End

Fig. 19

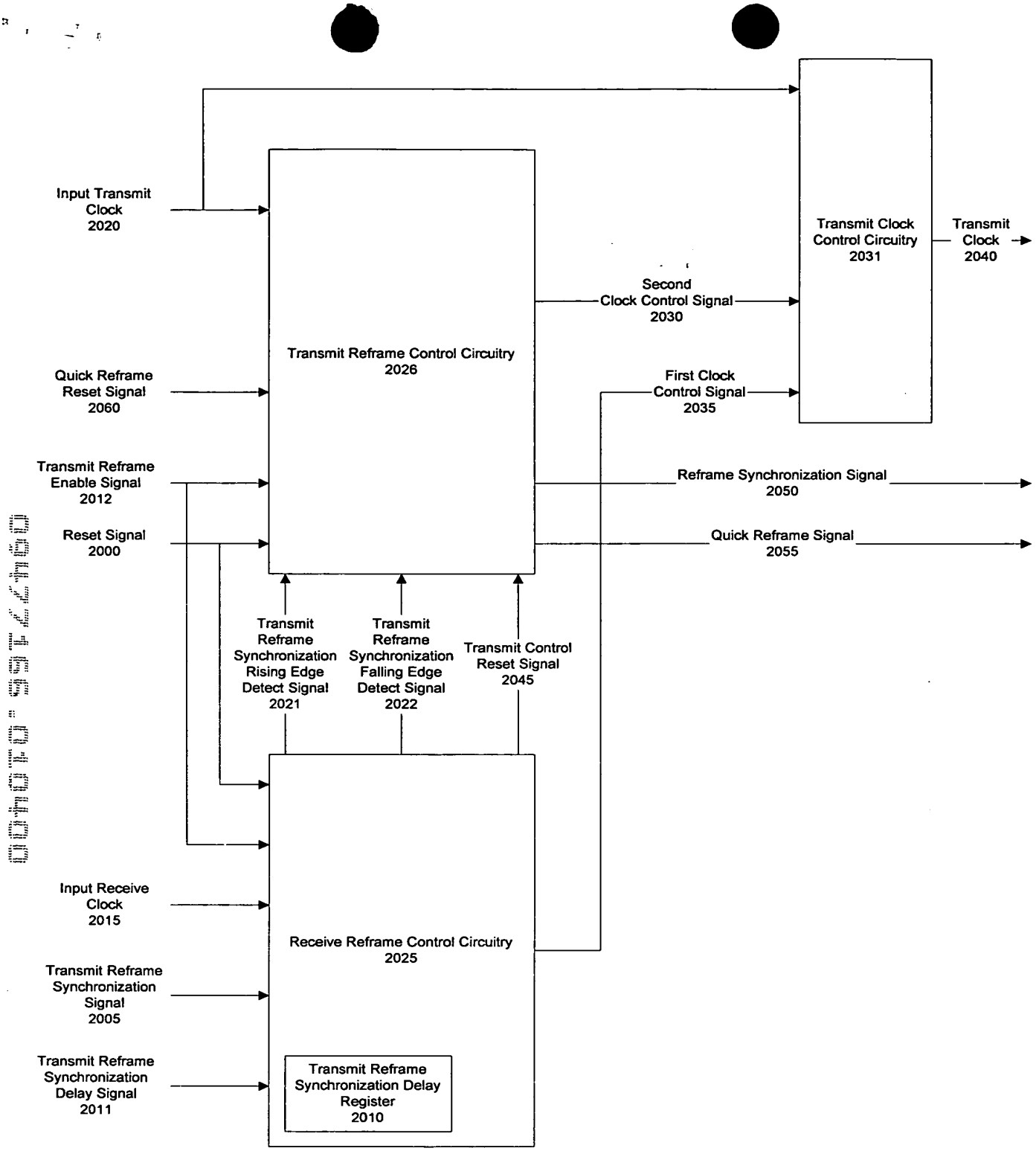
Input Transmit Clock 2020
Transmit Clock Control Circuitry 2031
Transmit Clock 2040
Second Clock Control Signal 2030
Transmit Reframe Control Circuitry 2026
Quick Reframe Reset Signal 2060
First Clock Control Signal 2035
Transmit Reframe Enable Signal 2012
Reframe Synchronization Signal 2050
Reset Signal 2000
Quick Reframe Signal 2055
Transmit Reframe Synchronization Rising Edge Detect Signal 2021
Transmit Reframe Synchronization Falling Edge Detect Signal 2022
Transmit Control Reset Signal 2045
Input Receive Clock 2015
Receive Reframe Control Circuitry 2025
Transmit Reframe Synchronization Signal 2005
Transmit Reframe Synchronization Delay Signal 2011
Transmit Reframe Synchronization Delay Register 2010

Fig. 20

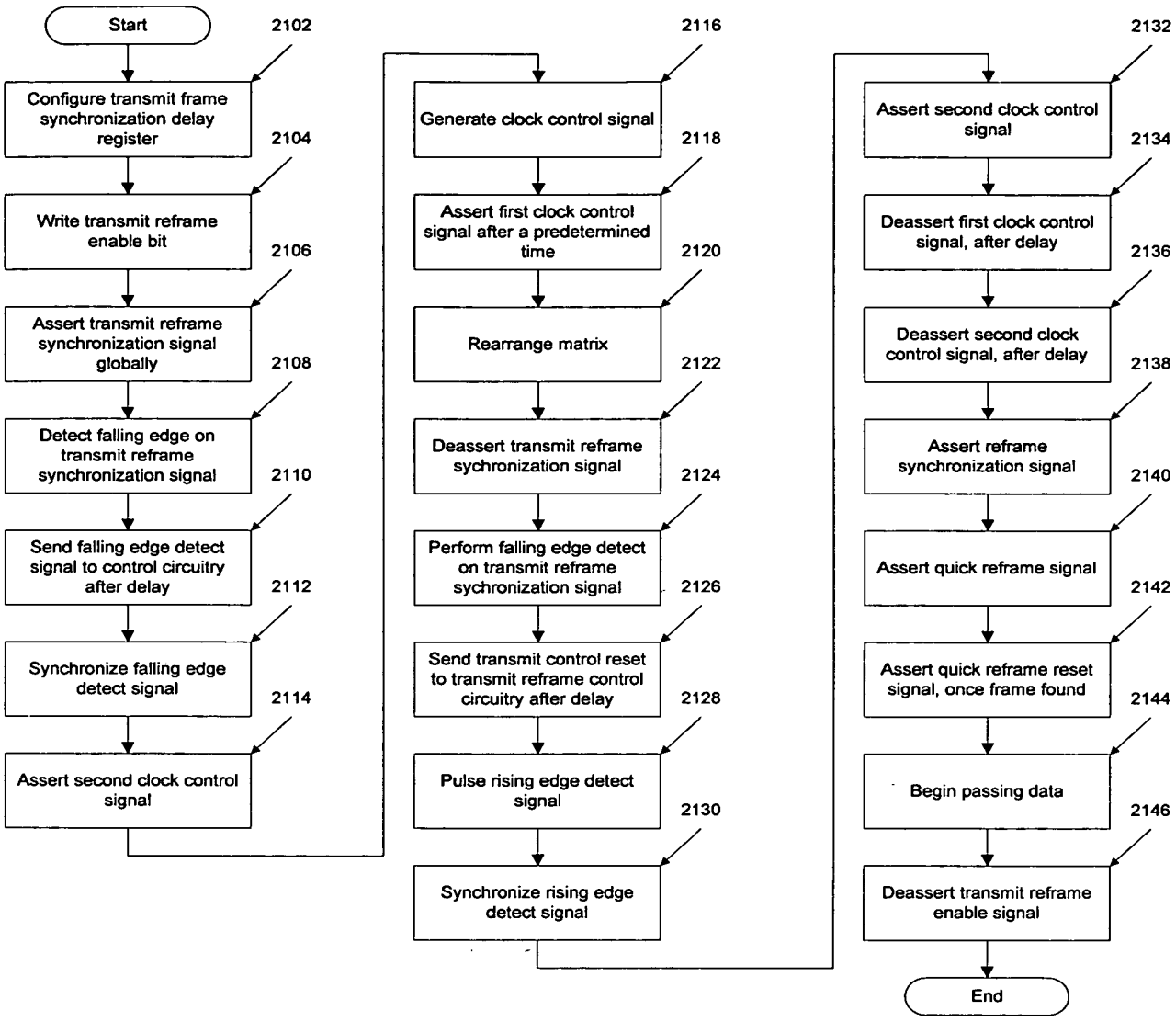
Start
2102
Configure transmit frame synchronization delay register
2104
Write transmit reframe enable bit
2106
Assert transmit reframe synchronization signal globally
2108
Detect falling edge on transmit reframe synchronization signal
2110
Send falling edge detect signal to control circuitry after delay
2112
Synchronize falling edge detect signal
2114
Assert second clock control signal
2116
Generate clock control signal
2118
Assert first clock control signal after a predetermined time
2120
Rearrange matrix
2122
Deassert transmit reframe sychronization signal
2124
Perform falling edge detect on transmit reframe sychronization signal
2126
Send transmit control reset to transmit reframe control circuitry after delay
2128
Pulse rising edge detect signal
2130
Synchronize rising edge detect signal
2132
Assert second clock control signal
2134
Deassert first clock control signal, after delay
2136
Deassert second clock control signal, after delay
2138
Assert reframe synchronization signal
2140
Assert quick reframe signal
2142
Assert quick reframe reset signal, once frame found
2144
Begin passing data
2146
Deassert transmit reframe enable signal
End

Fig. 21

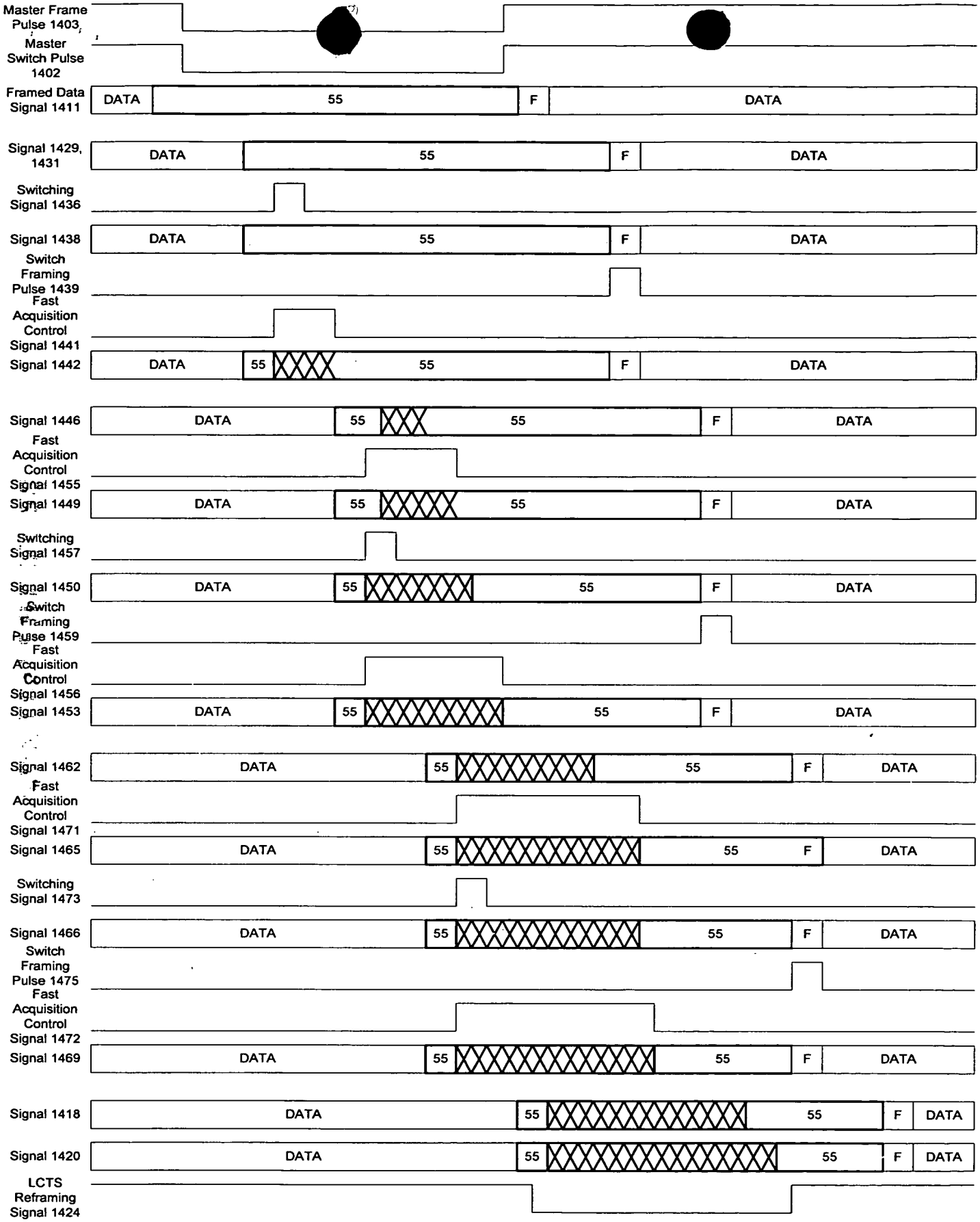
Master Frame Pulse 1403,
Master Switch Pulse 1402
Framed Data Signal 1411
DATA
55
F
DATA
Signal 1429, 1431
Switching Signal 1436
Signal 1438
Switch Framing Pulse 1439
Fast Acquisition Control Signal 1441
Signal 1442
Signal 1446
Fast Acquisition Control Signal 1455
Signal 1449
Switching Signal 1457
Signal 1450
Switch Framing Pulse 1459
Fast Acquisition Control Signal 1456
Signal 1453
Signal 1462
Fast Acquisition Control Signal 1471
Signal 1465
Switching Signal 1473
Signal 1466
Switch Framing Pulse 1475
Fast Acquisition Control Signal 1472
Signal 1469
Signal 1418
Signal 1420
LCTS Reframing Signal 1424

Fig. 17